Experiment No. 4: Multistage Amplifiers and Cascode Configuration

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1. Aim of the Experiment

To analyze the performance characteristics of multistage amplifiers, particularly two-stage RC coupled BJT amplifiers, and to understand the advantages and operation of the Cascode amplifier configuration, with a focus on high-frequency performance.

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2. Objectives

Upon successful completion of this experiment, students will be able to:

- Design and construct a two-stage RC coupled Common-Emitter (CE) BJT amplifier.
- Measure and verify the individual stage gains and overall voltage gain of a multistage amplifier.
- Plot the frequency response of a multistage amplifier and determine its overall bandwidth.
- Design and construct a BJT Cascode amplifier.
- Measure the voltage gain and frequency response of a Cascode amplifier.
- Compare the high-frequency performance (upper cutoff frequency and bandwidth) of a Cascode amplifier with that of a single-stage Common-Emitter amplifier.
- Explain the reasons behind the improved high-frequency response of a Cascode amplifier.

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3. Apparatus and Components Required

S. No.	Item	Specification / Type	Quantity
1.	DC Regulated Power Supply	0-30V, 1A (or similar)	1
2.	AC Function Generator	Sine wave, 1Hz - 1MHz (or higher)	1
3.	Digital Oscilloscope	Dual channel, 20MHz bandwidth (or higher)	1

4.	Digital Multimeter (DMM)	For DC voltage and resistance measurements	1
5.	Breadboard	Standard size	1
6.	NPN BJT	BC547 (or 2N3904, 2N2222, etc.)	3
7.	Resistors	Various standard E12/E24 series (e.g., 100Ω, 220Ω, 470Ω, 1kΩ, 2.2kΩ, 4.7kΩ, 10kΩ, 22kΩ, 47kΩ, 100kΩ, 470kΩ)	As per design
8.	Capacitors	Electrolytic (10$\muF,100\muF)andCeramic/Mylar(0.01\muF,0.1\mu$F)	As per design
9.	Connecting Wires	Assorted	As needed

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4. Theoretical Background

4.1. Multistage Amplifiers: The Need for Cascading

A single transistor amplifier stage typically provides a limited voltage gain. For applications requiring very high overall gain (e.g., in audio systems, sensor signal conditioning), a single stage is insufficient. To achieve higher overall gain, multiple amplifier stages are connected in cascade, meaning the output of one stage is connected to the input of the next stage. This arrangement forms a **multistage amplifier**.

Why Multistage Amplifiers are Used:

- **Increased Overall Gain:** The primary reason is to achieve a much higher total voltage gain than a single stage can provide.
- **Desired Input/Output Impedances:** Different stages can be designed with specific input and output impedance characteristics to meet system requirements. For instance, an initial stage might have high input impedance to avoid loading the source, while a final stage might have low output impedance to drive a low-impedance load.
- **Improved Frequency Response (though not inherently, careful design is needed):** While cascading stages generally reduces overall bandwidth, specific designs can optimize the frequency response.
- **Isolation:** Stages can provide some isolation between input and output, and between different parts of the circuit.

Types of Multistage Coupling: The way stages are connected (coupled) influences the amplifier's performance, especially its frequency response and DC biasing. Common coupling methods include:

- **RC Coupling:** Resistor-Capacitor coupling. This uses a coupling capacitor (CC) to block DC and pass AC between stages, and bypass capacitors (CE) to provide AC ground at the emitters/sources. It is cost-effective and common.
- **Direct Coupling:** Stages are directly connected without capacitors. This allows amplification of DC signals but makes biasing more complex as the DC Q-point of one stage affects the next.
- **Transformer Coupling:** Uses transformers to couple stages. Provides impedance matching and gain, but transformers are bulky, expensive, and have limited frequency response.

In this experiment, we will focus on **RC Coupled BJT Amplifiers** due to their widespread use and simplicity.

Overall Gain of Multistage Amplifiers: When multiple stages are cascaded, the overall voltage gain (AV(total)) is the product of the individual voltage gains of each stage, provided there are no significant loading effects between stages or if loading is accounted for in each stage's gain calculation.

$A_{V(total)} = A_{V1} \times A_{V2} \times A_{V3} \times ... \times A_{Vn}$ Where A_{Vn} is the voltage gain of the nth stage.

It is often expressed in decibels (dB): $A_{V(total),dB} = A_{V1,dB} + A_{V2,dB} + A_{V3,dB} + ... + A_{Vn,dB}$

Frequency Response of Multistage Amplifiers: The frequency response of a multistage amplifier is determined by the cumulative effect of all individual stages. The overall bandwidth of a multistage amplifier is generally *less* than the bandwidth of any individual stage. This is because any frequency where a single stage's gain starts to roll off will cause the overall gain to roll off even faster. The cutoff frequencies (lower fL and upper fH) of the overall amplifier will be affected by the dominant cutoff frequencies of the individual stages.

4.2. Cascode Amplifier Configuration

The Common-Emitter (CE) amplifier, while providing high gain, suffers from a limitation at high frequencies due to the **Miller Effect**.

Miller Effect: In a CE amplifier, there is a parasitic capacitance (C_{BC} or C_{CB}) between the collector and base of the BJT. Due to the voltage gain of the stage, this capacitance is effectively magnified at the input, creating a much larger input capacitance called the Miller capacitance (C_M). $C_M = C_{BC}(1+A_V)$ where A_V is the voltage gain of the CE stage. This magnified input capacitance significantly reduces the input impedance at high frequencies, causing the gain to roll off and limiting the amplifier's upper cutoff frequency (f_H).

The Cascode Solution: The **Cascode amplifier** configuration is designed specifically to mitigate the Miller effect and improve the high-frequency response of the amplifier. It combines a Common-Emitter (CE) stage with a Common-Base (CB) stage.

Configuration:

- The first transistor (Q1) is in a CE configuration. Its collector is directly connected to the emitter of the second transistor (Q2).
- The second transistor (Q2) is in a CB configuration. Its base is held at a fixed DC voltage (AC ground via a bypass capacitor), and its input is its emitter, connected to Q1's collector. Its output is taken from its collector.

How it Reduces Miller Effect: In the Cascode configuration:

- The first stage (Q1 - CE) has its collector connected directly to the emitter of the second stage (Q2 - CB). The voltage gain of the first stage, AV1, is very low (close to 1) because its load impedance is the very low input impedance of the CB stage.
- Since AV1 is very low, the Miller capacitance (CM=CBC1(1+AV1)) for Q1 is significantly reduced. This largely eliminates the Miller effect at the input of the overall amplifier.
- The second stage (Q2 - CB) provides the high voltage gain. Although it also has a CBC2, this capacitance is between the output (collector) and an AC grounded point (base), so it does not contribute to the Miller effect at the input.
- The overall voltage gain of the Cascode is approximately the product of the small gain of the CE stage and the large gain of the CB stage, resulting in high overall gain. The crucial benefit is that this high gain is achieved without the debilitating Miller effect at the input, leading to a significantly higher upper cutoff frequency and wider bandwidth.

Advantages of Cascode Amplifier:

- **Improved High-Frequency Response:** Significantly reduces Miller effect, leading to higher bandwidth and upper cutoff frequency (fH).
- **High Voltage Gain:** Combines the high gain of the CB stage with the isolation of the CE stage.
- **Good Input-Output Isolation:** The common-base stage provides excellent isolation between the input and output.

Disadvantages of Cascode Amplifier:

- Requires two transistors, increasing complexity and cost.
- Requires higher supply voltage due to voltage drops across two transistors.

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5. Pre-Lab Design and Calculations

5.1. Two-Stage RC Coupled BJT Amplifier Design (Common-Emitter Stages)

We will design two identical CE stages and then cascade them. Assume biasing will be done using the Voltage Divider Bias scheme (as learned in Experiment 2) for stability.

Common Parameters for Each Stage:

- Supply Voltage: VCC=12V
- Transistor: NPN BJT (BC547)

- Assume βDC for BC547 = 100
- Assume VBE=0.7V
- Target Q-point for each stage: IC=1mA, VCE=6V

Design for a Single CE Stage (Voltage Divider Bias):

1. **Target IC=1mA, VCE=6V.**
2. **Calculate VE and RE:**
    - Let VE≈0.15×VCC=0.15×12V=1.8V.
    - RE=IEVE≈ICVE=1mA1.8V=1.8kΩ.
    - **Choose Standard RE:** 1.8kΩ.
    - Recalculated VE=1mA×1.8kΩ=1.8V.
3. **Calculate VC and RC:**
    - VC=VCE+VE=6V+1.8V=7.8V.
    - RC=ICVCC−VC=1mA12V−7.8V=1mA4.2V=4.2kΩ.
    - **Choose Standard RC:** 4.2kΩ (or 4.3kΩ for E24 series). Let's use 4.3kΩ.
    - Recalculated VC=12V−(1mA×4.3kΩ)=12V−4.3V=7.7V.
    - Recalculated VCE=7.7V−1.8V=5.9V. (Close to target 6V).
4. **Calculate VB:**
    - VB=VE+VBE=1.8V+0.7V=2.5V.
5. **Calculate R1 and R2 (Voltage Divider):**
    - IB=βDCIC=1001mA=10μA.
    - Choose IR2=10×IB=10×10μA=100μA.
    - R2=IR2VB=100μA2.5V=25kΩ.
    - **Choose Standard R2:** 22kΩ.
    - R1=IR2+IBVCC−VB=100μA+10μA12V−2.5V=110μA9.5V≈86.36kΩ.
    - **Choose Standard R1:** 82kΩ or 91kΩ. Let's use 82kΩ.

DC Biasing Summary for Each CE Stage:

- R1=82kΩ
- R2=22kΩ
- RC=4.3kΩ
- RE=1.8kΩ

AC Analysis for a Single CE Stage (Voltage Gain):

The voltage gain of a CE amplifier is approximately: AV=−re′RC∣∣RL Where:

- RC is the collector resistor.
- RL is the effective AC load seen by the collector. For the first stage, RL will be the input impedance of the second stage. For the second stage, RL will be the actual external load (e.g., oscilloscope probe impedance, which is high, or a specified load resistor).
- re′ is the AC emitter resistance, calculated as re′=IE25mV.
    - IE≈IC=1mA. So, re′=1mA25mV=25Ω.

Coupling Capacitors (CC) and Bypass Capacitor (CE): These capacitors are chosen to have a very low impedance at the operating frequency range.

- **CC (Coupling Capacitor):** Blocks DC bias from previous/next stages. Its value affects the lower cutoff frequency (fL). Choose a large enough value (e.g., 1µF to 10µF) such that XC is much smaller than the input impedance of the next stage at fL. A common practice is to choose CC such that Rin,stage≈2πfLCC1.
- **CE (Emitter Bypass Capacitor):** Bypasses RE at AC frequencies to prevent negative feedback that would reduce gain. Its value also affects fL. Choose a large enough value (e.g., 10µF to 100µF) such that XCE is much smaller than re′ at fL. A common practice is RE∣∣(re′+βRin,source)≈2πfLCE1.

Let's assume a desired lower cutoff frequency (fL) of approximately 100 Hz.

Calculation of Coupling Capacitors (CC1, CC2):

- Rin(stage2) (Input impedance of the second stage) = R1∣∣R2∣∣(βACre′).
    - Assuming βAC≈βDC=100.
    - Rin(stage2)=82kΩ∣∣22kΩ∣∣(100×25Ω)=82kΩ∣∣22kΩ∣∣2.5kΩ.
    - 82kΩ∣∣22kΩ≈17.2kΩ.
    - Rin(stage2)≈17.2kΩ∣∣2.5kΩ≈2.18kΩ.
- For CC1 (between input source and Stage 1): CC1≈2πfLRin(stage1)1. Since input source impedance is usually low, CC1 needs to be large. Let Rin(stage1) be the calculated Rin(stage2). CC1≈2π(100Hz)(2.18kΩ)1≈0.73µF. **Choose CC1=1µF or 2.2µF. Let's use 1µF.**
- For CC2 (between Stage 1 output and Stage 2 input): Rout(stage1)≈RC=4.3kΩ. This will be in series with Rin(stage2). CC2≈2πfL(Rout(stage1)+Rin(stage2))1=2π(100Hz)(4.3kΩ+2.18kΩ)1=2π(100Hz)(6.48kΩ)1≈0.24µF. **Choose CC2=0.47µF or 1µF. Let's use 1µF.**

Calculation of Emitter Bypass Capacitors (CE):

- For CE (across RE): Rth(emitter)=RE∣∣(re′+βACRTH,Base). RTH,Base is the Thevenin resistance of the base voltage divider. RTH,Base=R1∣∣R2=82kΩ∣∣22kΩ≈17.2kΩ. Rth(emitter)≈re′+βACRTH,Base=25Ω+10017200Ω=25Ω+172Ω=197Ω. CE≈2πfLRth(emitter)1=2π(100Hz)(197Ω)1≈8.08µF. **Choose CE=10µF or 22µF. Let's use 10µF.**

Gain Calculation for Two-Stage Amplifier:

- **Stage 1 Gain (AV1):**
    - Load for Stage 1 is RC in parallel with Rin(stage2).
    - RL1(eff)=RC∣∣Rin(stage2)=4.3kΩ∣∣2.18kΩ≈1.44kΩ.
    - AV1=−re′RL1(eff)=−25Ω1440Ω=−57.6.
- **Stage 2 Gain (AV2):**
    - Load for Stage 2 is RC (assuming high output impedance of oscilloscope as load).
    - RL2(eff)=RC=4.3kΩ.
    - AV2=−re′RL2(eff)=−25Ω4300Ω=−172.
- **Overall Gain (AV(total)):**
    - AV(total)=AV1×AV2=(−57.6)×(−172)=9916.8.

- AV(total),dB=20log10(9916.8)≈79.9dB.

Summary of Components for Two-Stage RC Coupled BJT Amplifier:

- **Transistors:** Q1, Q2 (BC547)
- **Resistors (for each stage):**
  - R1=82kΩ
  - R2=22kΩ
  - RC=4.3kΩ
  - RE=1.8kΩ
- **Capacitors:**
  - CC1 (Input Coupling) = 1µF
  - CC2 (Inter-stage Coupling) = 1µF
  - CC3 (Output Coupling) = 1µF (Similar calculation for CC1 but for output load).
  - CE1 (Emitter Bypass for Q1) = 10µF
  - CE2 (Emitter Bypass for Q2) = 10µF

Calculated Theoretical Q-points (for each stage):

- IC=[1mA]
- VCE=[5.9V]

Calculated Theoretical Gains:

- AV1=[−57.6]
- AV2=[−172]
- AV(total)=[9916.8] or [79.9dB]

5.2. Cascode Amplifier Design

Given Parameters:

- Supply Voltage: VCC=12V
- Transistors: NPN BJT (BC547) - Q1 (CE), Q2 (CB)
- Assume βDC=100, VBE=0.7V.
- Let's aim for the same quiescent collector current as the previous stage: IC=1mA.

Design Steps:

1. **Biasing Q1 (Common-Emitter part):**
   - Use Voltage Divider Bias for Q1, similar to the previous single stage.
   - Target IC=1mA.
   - RE1=1.8kΩ (for VE1=1.8V)
   - R1=82kΩ, R2=22kΩ (sets VB1≈2.5V).
   - **Note:** Q1's collector is connected to Q2's emitter, so there's no RC1 in the traditional sense here.
2. **Biasing Q2 (Common-Base part):**
   - The emitter of Q2 is biased by the collector of Q1. So IE2≈IC1≈1mA.
   - The base of Q2 needs a stable DC voltage for the CB configuration. This is typically achieved using a voltage divider from VCC.

    - Let VB2 be chosen such that VC1=VE2=VB2−VBE2.
    - We want VC1 (collector of Q1) to be high enough for Q1 to be in the active region (e.g., VCE1≈3V to 4V).
    - If VC1=4V, then VB2=VC1+VBE2=4V+0.7V=4.7V.
    - Design a voltage divider for VB2: R3 and R4 (from VCC to ground).
        - Let the current through this divider be IR4=10×IB2=10×(IC2/β)=10×(1mA/100)=100μA.
        - R4=IR4VB2=100μA4.7V=47kΩ. **Choose R4=47kΩ.**
        - R3=IR4+IB2VCC−VB2=100μA+10μA12V−4.7V=110μA7.3V≈66.36kΩ. **Choose R3=68kΩ.**
    - A bypass capacitor (CB2) from VB2 to ground is needed to provide an AC ground at the base of Q2.
        - CB2≈2πfL(R3∣∣R4)1. Assuming fL=100Hz.
        - R3∣∣R4=68kΩ∣∣47kΩ≈27.8kΩ.
        - CB2≈2π(100Hz)(27.8kΩ)1≈0.057μF. **Choose CB2=0.1μF.**
3. **Collector Resistor for Q2 (RC2):**
    - This sets the output Q-point for the Cascode amplifier.
    - Target VCE2=VDD/2=6V.
    - VC2=VCE2+VE2=6V+VC1=6V+4V=10V.
    - RC2=IC2VCC−VC2=1mA12V−10V=1mA2V=2kΩ.
    - **Choose Standard RC2:** 2kΩ or 2.2kΩ. Let's use 2.2kΩ.

DC Biasing Summary for Cascode Amplifier:

- Q1: R1=82kΩ, R2=22kΩ, RE1=1.8kΩ
- Q2: R3=68kΩ, R4=47kΩ, RC2=2.2kΩ
- Capacitors: CC1 (input) = 1μF, CE1 (Q1 emitter bypass) = 10μF, CB2 (Q2 base bypass) = 0.1μF, CC3 (output coupling) = 1μF.

AC Analysis for Cascode Amplifier (Voltage Gain):

- The effective AC load for Q1 (CE stage) is the input impedance of Q2 (CB stage). The input impedance of a CB stage is very low, approximately re′=25Ω.
- So, AV1≈−re′re′=−1. (This confirms the low gain of the first stage, which is key to reducing Miller effect).
- The overall gain of the Cascode is primarily determined by the CB stage's gain.
- AV(Cascode)≈−re′RC2 (The negative sign indicates phase inversion for the common-base part as well, due to the connection).
    - Using re′=25Ω and RC2=2.2kΩ.
    - AV(Cascode)=−25Ω2200Ω=−88.
    - AV(Cascode),dB=20log10(88)≈38.89dB.

Calculated Theoretical Q-points (for Cascode):

- IC=[1mA] (for both Q1 and Q2)
- VCE1≈[4V−1.8V=2.2V]
- VCE2≈[10V−4V=6V]

Calculated Theoretical Gain (Cascode):

- AV(Cascode)=[−88] or [38.89dB]

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6. Circuit Diagrams

(Draw these clearly in your practical file. Use standard component symbols and label all components with their calculated values.)

6.1. Two-Stage RC Coupled BJT Amplifier Circuit

[**Drawing Space:** A clear, labeled diagram of the two-stage NPN BJT RC Coupled Common-Emitter amplifier.

- Show VCC at the top.
- Stage 1: R1,R2,RC,RE for Q1, CE1.
- Input coupling capacitor CC1 to Q1 base.
- Inter-stage coupling capacitor CC2 from Q1 collector to Q2 base.
- Stage 2: R1,R2,RC,RE for Q2, CE2.
- Output coupling capacitor CC3 from Q2 collector to Output.
- Label all resistors, capacitors, and transistor terminals (Emitter, Base, Collector). Show ground connections clearly.]

6.2. Cascode Amplifier Circuit

[**Drawing Space:** A clear, labeled diagram of the NPN BJT Cascode amplifier.

- Show VCC at the top.
- Q1 (CE stage): R1,R2 (for base bias), RE1, CE1 (emitter bypass).
- Input coupling capacitor CC1 to Q1 base.
- Q2 (CB stage): R3,R4 (for base bias), CB2 (base bypass to AC ground).
- Collector of Q1 directly connected to emitter of Q2.
- RC2 from VCC to collector of Q2.
- Output coupling capacitor CC3 from Q2 collector to Output.
- Label all resistors, capacitors, and transistor terminals. Show ground connections clearly.]

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7. Procedure

7.1. Two-Stage RC Coupled BJT Amplifier Implementation and Gain Measurement

1. **Collect Components:** Gather all resistors and capacitors as per Section 5.1 design. Get two NPN BJTs (BC547).
2. **Construct Circuit:** Carefully assemble the two-stage RC coupled BJT amplifier on the breadboard as per your circuit diagram (Section 6.1). Double-check all connections.
3. **Power On:** Connect the DC power supply to VCC (12V) and ground. **Ensure the power supply is OFF before connecting.**

4. **Initial DC Check:** Before applying AC input, turn on the DC power supply and measure the DC Q-point voltages for each transistor: VC,VB,VE for Q1 and Q2. Record these in Table 10.1.1. Calculate IC and VCE for each stage. Compare with theoretical values.
5. **Apply AC Input:**
    - Set the Function Generator to generate a sine wave.
    - Choose a mid-band frequency (e.g., 1kHz) where the gain is expected to be relatively flat.
    - Set the input voltage (Vin) to a small amplitude (e.g., 20mV peak-to-peak or 10mV RMS) to ensure the amplifier operates in its linear region without clipping. Connect the Function Generator output to the input of the first stage (via CC1).
6. **Measure Individual Stage Gains:** Use the Oscilloscope to measure the AC peak-to-peak (or RMS) voltages.
    - **Stage 1 Gain (AV1):**
        - Connect Channel 1 of the oscilloscope to the input (Vin) of the first stage (before CC1, or at the base of Q1 after CC1).
        - Connect Channel 2 of the oscilloscope to the output of the first stage (collector of Q1, before CC2).
        - Measure Vin and Vout1 (output of stage 1). Calculate AV1=Vout1/Vin. Note the phase relationship. Record in Table 10.1.2.
    - **Stage 2 Gain (AV2):**
        - Connect Channel 1 to the input of the second stage (base of Q2, after CC2).
        - Connect Channel 2 to the output of the second stage (collector of Q2, before CC3).
        - Measure Vin2 (input to stage 2) and Vout2 (output of stage 2). Calculate AV2=Vout2/Vin2. Note the phase relationship. Record in Table 10.1.2.
7. **Measure Overall Gain (AV(total)):**
    - Connect Channel 1 of the oscilloscope to the overall input (Vin) of the first stage.
    - Connect Channel 2 of the oscilloscope to the overall output (Vout) of the second stage (after CC3).
    - Measure Vin and Vout. Calculate AV(total)=Vout/Vin. Note the phase relationship. Record in Table 10.1.2.
8. **Compare Gains:** Compare the measured overall gain with the product of the individual stage gains (AV1×AV2). Record in Table 10.1.2.
9. **Power Off:** Turn off the DC power supply and Function Generator.

7.2. Multistage Frequency Response Plotting

1. **Set up Measurement:** Ensure the two-stage amplifier is connected as for overall gain measurement (Input Channel 1, Output Channel 2).
2. **Mid-band Gain Reference:** From previous steps, you have the overall gain (AV(mid)) at 1kHz. Convert this to dB: AV(mid),dB=20log10(AV(mid)).
3. **Find Lower Cutoff Frequency (fL):**

    - Start with the mid-band frequency. Slowly decrease the input frequency from the Function Generator.
    - Monitor the output voltage on the oscilloscope. The output voltage will start to decrease as frequency goes down.
    - The lower cutoff frequency (fL) is reached when the output voltage drops to 0.707×Vout(mid) (or −3dB from mid-band gain). Record fL in Table 10.2.1.
4. **Find Upper Cutoff Frequency (fH):**
    - Return to the mid-band frequency. Slowly increase the input frequency from the Function Generator.
    - Monitor the output voltage. The output voltage will start to decrease as frequency goes up.
    - The upper cutoff frequency (fH) is reached when the output voltage drops to 0.707×Vout(mid) (or −3dB from mid-band gain). Record fH in Table 10.2.1.
5. **Determine Bandwidth (BW):**
    - Calculate Bandwidth = fH−fL. Record in Table 10.2.1.
6. **Plot Frequency Response:**
    - Take readings of output voltage (or gain in dB) at various frequencies across the entire spectrum (from very low to very high, spanning well beyond fL and fH). Record in Table 10.2.2.
    - Plot the Gain (in dB) vs. Frequency (on a logarithmic scale) on a semi-log graph paper.

7.3. Cascode Amplifier Implementation and Measurement

1. **Collect Components:** Gather all resistors and capacitors as per Section 5.2 design. Get two NPN BJTs (BC547).
2. **Construct Circuit:** Carefully assemble the BJT Cascode amplifier on the breadboard as per your circuit diagram (Section 6.2). Double-check all connections.
3. **Power On:** Connect the DC power supply to VCC (12V) and ground.
4. **Initial DC Check:** Turn on DC power supply and measure DC voltages: VC2,VB2,VE2(VC1),VB1,VE1. Record these in Table 10.3.1. Compare with theoretical values.
5. **Apply AC Input:**
    - Set the Function Generator to generate a sine wave at a mid-band frequency (e.g., 1kHz).
    - Set the input voltage (Vin) to a small amplitude (e.g., 20mV peak-to-peak). Connect to the input of the Cascode.
6. **Measure Voltage Gain:**
    - Connect Channel 1 of the oscilloscope to the input (Vin).
    - Connect Channel 2 of the oscilloscope to the output (Vout).
    - Measure Vin and Vout. Calculate AV(Cascode)=Vout/Vin. Record in Table 10.3.2.
7. **Plot Cascode Frequency Response:**
    - Repeat the frequency response plotting procedure (similar to 7.2) for the Cascode amplifier.
    - Determine its lower cutoff frequency (fL), upper cutoff frequency (fH), and bandwidth. Record in Table 10.3.2.

- Take readings of output voltage (or gain in dB) at various frequencies across the spectrum. Record in Table 10.3.3.
- Plot the Gain (in dB) vs. Frequency (on a logarithmic scale).

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10. Observations and Readings

10.1. Two-Stage RC Coupled BJT Amplifier Readings

Designed Component Values (Each Stage):

- $R_1 = $ [Value]
- $R_2 = $ [Value]
- $R_C = $ [Value]
- $R_E = $ [Value]
- $C_{C1} = $ [Value], $C_{C2} = $ [Value], $C_{C3} = $ [Value]
- $C_{E1} = $ [Value], $C_{E2} = $ [Value]

Table 10.1.1: DC Q-point Measurements for Two-Stage Amplifier

Parameter	Theoretical (Q1)	Measured (Q1)	Theoretical (Q2)	Measured (Q2)
VB	[from 5.1]		[from 5.1]	
VE	[from 5.1]		[from 5.1]	
VC	[from 5.1]		[from 5.1]	
IC (Calculated)	[from 5.1]		[from 5.1]	
VCE (Calculated)	[from 5.1]		[from 5.1]	

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Table 10.1.2: Two-Stage Amplifier Gain Measurements (at mid-band, e.g., 1kHz)

Parameter	Theoretical (Magnitude)	Measured (Magnitude)	Measured (dB)	Phase Shift (Measured)
Input Voltage (Vin)	N/A		N/A	N/A
Vout1 (Stage 1)	N/A		N/A	N/A
AV1	[from 5.1]			
Vin2 (Stage 2 Input)	N/A		N/A	N/A
Vout2 (Overall Output)	N/A		N/A	N/A

AV2	[from 5.1]	
AV(total) (Measured Overall)	N/A	
AV1×AV2 (Product of Individual)	[from 5.1]	N/A

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10.2. Multistage Frequency Response Readings

Table 10.2.1: Multistage Amplifier Cutoff Frequencies and Bandwidth

Parameter	Value (Hz)
Mid-band Frequency (fmid)	1kHz
Mid-band Gain (Measured dB)	
Lower Cutoff Frequency (fL)	
Upper Cutoff Frequency (fH)	
Bandwidth (BW=fH−fL)	

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Table 10.2.2: Multistage Amplifier Frequency Response Data

Frequency (Hz)	Input Voltage (Vin p-p)	Output Voltage (Vout p-p)	Gain (Vout/Vin)	Gain (dB) = 20log10(Gain)
... (start from low freq)				
10				
50				
100				
500				
1k (mid-band)				
5k				
10k				
50k				
100k				

... (to high freq)

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10.3. Cascode Amplifier Readings

Designed Component Values (Cascode):

- $R_1 = $ [Value], $R_2 = $ [Value], $R_{E1} = $ [Value]
- $R_3 = $ [Value], $R_4 = $ [Value], $R_{C2} = $ [Value]
- $C_{C1} = $ [Value], $C_{E1} = $ [Value], $C_{B2} = $ [Value], $C_{C3} = $ [Value]

Table 10.3.1: DC Q-point Measurements for Cascode Amplifier

Parameter	Theoretical (Q1)	Measured (Q1)	Theoretical (Q2)	Measured (Q2)
VB	[from 5.2]		[from 5.2]	
VE	[from 5.2]		[from 5.2]	
VC	[from 5.2]		[from 5.2]	
IC (Calculated)	[from 5.2]		[from 5.2]	
VCE (Calculated)	[from 5.2]		[from 5.2]	

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Table 10.3.2: Cascode Amplifier Gain and Bandwidth (at mid-band, e.g., 1kHz)

Parameter	Theoretical (Magnitude)	Measured (Magnitude)	Measured (dB)	Phase Shift (Measured)
Input Voltage (Vin)	N/A		N/A	N/A
Output Voltage (Vout)	N/A		N/A	N/A
AV(Cascode)	[from 5.2]			
Mid-band Frequency (fmid)	1kHz	N/A	N/A	N/A
Lower Cutoff Frequency (fL)	N/A		N/A	N/A
Upper Cutoff Frequency (fH)	N/A		N/A	N/A
Bandwidth (BW=fH−fL)	N/A		N/A	N/A

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Table 10.3.3: Cascode Amplifier Frequency Response Data

Frequency (Hz)	Input Voltage (Vin p-p)	Output Voltage (Vout p-p)	Gain (Vout/Vin)	Gain (dB) = 20log10(Gain)
...				
10				
...				
1k (mid-band)				
...				
100k				
500k				
1M				
...				

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11. Calculations

(Show all detailed calculations here. Include AC gain calculations using actual measured DC Q-points if they significantly differ from theoretical.)

11.1. Two-Stage RC Coupled BJT Amplifier Calculations:

- **DC Q-point calculations for each stage:** Use the standard resistor values and measured DC voltages to confirm actual Q-points.
- **Individual Stage Gain Calculations:** Use measured AC voltages to calculate AV1 and AV2.
- **Overall Gain Calculation:** Calculate AV(total) from measured overall Vin and Vout.
- **Product of Individual Gains:** Calculate AV1×AV2. Compare with measured AV(total).
- **Bandwidth Calculation:** Show fH−fL.

11.2. Cascode Amplifier Calculations:

- **DC Q-point calculations:** Use standard resistor values and measured DC voltages to confirm actual Q-points for Q1 and Q2.
- **Voltage Gain Calculation:** Use measured AC voltages to calculate AV(Cascode). Compare with theoretical.
- **Bandwidth Calculation:** Show fH−fL.

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12. Results and Discussion

(Analyze your observations and calculations thoroughly here.)

12.1. Two-Stage RC Coupled BJT Amplifier:

- **DC Bias:** Discuss how closely your measured DC Q-points match the theoretical design values. Explain any discrepancies (e.g., resistor tolerances, β variations, DMM accuracy).
- **Gain Analysis:**
    - Compare the measured individual stage gains (AV1, AV2) with their theoretical values.
    - Compare the measured overall gain (AV(total)) with the product of individual stage gains (AV1×AV2). Are they approximately equal? Discuss any reasons for minor differences (e.g., loading effects not perfectly accounted for, measurement errors).
- **Frequency Response:**
    - Describe the shape of the frequency response curve for the two-stage amplifier.
    - State the measured lower (fL) and upper (fH) cutoff frequencies and the bandwidth.
    - Discuss how the coupling and bypass capacitors affect the lower cutoff frequency.
    - Discuss how the internal parasitic capacitances of the transistors affect the upper cutoff frequency.

12.2. Cascode Amplifier vs. Single-Stage Common-Emitter Performance:

- **(Refer to your Lab Experiment 3 data for Single-Stage CE, if available, or state assumptions for a typical CE amplifier's fH based on common knowledge/previous labs.)**
- **Gain:** Compare the mid-band voltage gain of the Cascode amplifier with that of a single Common-Emitter stage.
- **High-Frequency Performance:**
    - Compare the measured upper cutoff frequency (fH) and bandwidth (BW) of the Cascode amplifier with that of a typical single-stage Common-Emitter amplifier (e.g., from Lab Experiment 3, or a standard example).
    - **Crucially, explain in detail *why* the Cascode configuration exhibits a superior high-frequency response.** Focus on how it effectively minimizes the Miller effect in the input transistor (Q1), leading to a much wider bandwidth compared to a standard CE stage with similar gain.

12.3. Advantages and Disadvantages:

- **Multistage Amplifiers (General):**
    - **Advantages:** [List benefits observed/discussed, e.g., high gain].

    - **Disadvantages:** [List drawbacks, e.g., reduced overall bandwidth compared to individual stage bandwidths, increased complexity].
- **Cascode Amplifier:**
    - **Advantages:** [List specific benefits, e.g., excellent high-frequency response, high gain, good isolation].
    - **Disadvantages:** [List drawbacks, e.g., requires two transistors, potentially higher supply voltage needed].

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13. Conclusion

Summarize the key findings of the experiment. Reiterate the effectiveness of cascading stages for achieving high overall gain and the importance of the Cascode configuration in overcoming the Miller effect to achieve superior high-frequency performance. Conclude on the practical applications and trade-offs involved in designing multistage and cascode amplifiers.

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14. Viva-Voce Questions (For Instructor/Self-Study)

1. What is the main reason for cascading amplifier stages?
2. How is the overall voltage gain of a multistage amplifier calculated from the individual stage gains?
3. Why is the bandwidth of a multistage amplifier typically less than the bandwidth of any single stage?
4. Explain the Miller effect in the context of a Common-Emitter amplifier. Why is it problematic at high frequencies?
5. Draw the basic configuration of a Cascode amplifier and identify the type of configuration for each transistor.
6. How does the Cascode configuration reduce the Miller effect?
7. What is the approximate voltage gain of the first stage (CE) in a Cascode amplifier? Why is it so low?
8. Besides improved high-frequency response, what are other advantages of a Cascode amplifier?
9. What are the main disadvantages of a Cascode amplifier?
10. If you needed an amplifier with extremely high gain at very low frequencies, but poor high-frequency response was acceptable, what type of coupling would you choose for a multistage amplifier? Why?